Master/CivIng. Thesis Proposal 30 hp

Programmable Packet Scheduling in P4

Quality of Service (QoS) and in particular, resource sharing are important parts of the network research area, and QoS is still listed as a key issue for 5G standardization. An ideal resource sharing technique has to be lightweight, allow rich resource sharing policies. It has to be simple to implement and it must be able to fulfil predefined delay requirements. In the past ten years, various packet marking-based resource sharing approaches have been proposed from Core Stateless Fair Queueing and Rainbow Fair Queueing to Per Packet Value, sharing the idea that the packets are labeled at edge nodes of the network by applying predefined operator policies and then the resource nodes inside the network can solely schedule or drop packets according to the packet labels. These approaches provide lightweight solutions to control bandwidth sharing among flows even when per flow queuing is not possible.

Recently, the packet marking-based bandwidth sharing control of PPV has been combined with a lightweight proactive mechanism similar to PIE that reacts to congestion situations earlier than when buffers are filled up and ensures the bandwidth share defined by the marking policy between flows. This concept is called Packet Value-aware PIE (PVPIE) works in two stages: 1) the algorithm of PIE is applied to determine the expected drop probability needed to keep a target buffering delay; 2) the drop probability is translated to a Packet Value threshold that is then used to filter out incoming packets with Packet Value less than this threshold. The goal of PVPIE AQM is to keep the queuing delay at the target level and in parallel ensure the predefined resource sharing policies at any congestion level.

In this project work, you will extend a prototype of a PVPIE scheduler that has been implemented on a programmable switch using the P4 language. The main concept of this implementation is that the control plane is implemented in Python/C and interacts with the data plane that is implemented in P4 language. The control plane periodically reads Packet Value statistics from the data plane and updates drop thresholds. In order to extend the protoype, you will support multiple queues per output port, supporting different latency targets. In order to evaluate the prototype, you will define different traffic characteristics, create different traffic profiles and evaluate the latency and throughput characteristics based on different control loop cycles. This includes scalability aspects for scaling the algorithm to support multiple ports of the switch. Finally, you implement and evaluate an adaptive algorithm that updates the dropping thresholds based on traffic characteristics.

More information:

- P4: check the online course DVAD40 https://hhk3.kau.se/dpp/
- Packet Value concept: PVPIE: Take your own share of the PIE, available at https://irtf.org/anrw/2017/anrw17-final8.pdf

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