In Network Caching with P4

In this thesis, you develop a new key-value store architecture that leverages the power and flexibility of new-generation programmable network cards and switches to handle queries on hot items and balance the load across storage nodes. Your architecture should provide high aggregate throughput and low latency even under highly-skewed and rapidly-changing workloads. Using programmable switches and network cards with P4, you should efficiently detect, index, cache and serve hot key-value items in the switch data plane. Additionally, your solution should guarantee cache coherence with minimal overhead.

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